Study on SONOS Nonvolatile Memory Technology Using High-Density Plasma CVD Silicon Nitride

T. C. Chang, a,b,c S. T. Yan, b P. T. Liu, c C. W. Chen, b Y. C. Wu, b and S. M. Sze b,c

a Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan
b Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan
c National Nano Device Laboratory, Hsin-Chu 300, Taiwan


With the replacement of silicon nitride in an oxide/nitride/oxide (ONO) gate-stacked structure, trap-rich high-density plasma chemical vapor deposited (HDPCVD) SiNx shows a more significant threshold-voltage shift (memory window) than that of conventional low pressure (LP) CVD SiN x. Also, low-temperature (200°C) deposited HDPCVD silicon nitride shows a good retention characteristic, the same as high-temperature (780°C) LPCVD SiN x. With the optimization of thickness in the gate-stacked ONO structure, low-voltage and reliable operation, lower than 5 V, is realizable.

The Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates the difficult challenge, beyond the year 2005, for nonvolatile semiconductor memories is to achieve reliable, low-power, low-voltage performance.1 In the electrically erasable-programmable-read-only-memory (EEPROM) semiconductor device area, there are essentially two dominant technologies which compete for an ever-expanding world market: (i) floating gate EEPROMs and (ii) silicon/oxide/nitride/oxide/silicon (SONOS) (historically metal-nitride-oxide-silicon, MNOS) or floating-trap EEPROMs. The triple-dielectric SONOS structure (poly-Si gate/blocking oxide/silicon nitride/tunnel oxide/silicon substrate) is an attractive candidate for high density EEPROMs suitable for semiconductor disks and a replacement for high-density dynamic random memories (DRAMs).2 An advantage of the SONOS device over the floating-gate device is its improved endurance, because a single defect will not cause discharge of the memory.3 However, SONOS memories hardly reach a data retention for 10 years. This is why the actual use of SONOS memories is limited to military applications needing a high radiation hardness.4 When a memory device with a larger memory window is compared with a smaller one, it is easier to meet the requirement of retention of 10 years. This feature means that a memory device with a larger memory window will still possess an obvious difference of the threshold voltage ($\Delta V_T$) higher than the detecting limit of a typical sense amplifier while the memory device with a smaller memory window may lose its window in 10 years. A premise for this attention is that the leakage behavior of the memory device should be well tolerable. In this article, to provide a larger memory window to improve data retention, we introduce high-density plasma chemical vapor deposition (HDPCVD) silicon nitride to replace conventional low-pressure chemical vapor deposition (LPCVD) silicon nitride of the SONOS structure. A significant threshold-voltage shift due to charge trapping in the HDPCVD SiNx is observed with low leakage current of the ONO gate stack.

Experimental

The ONO gate-stacked structure in this study is shown in the inset of Fig. 1a. First, a 2 nm thermal oxide was grown on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace as a tunnel oxide. Subsequently, a 15 nm HDPCVD silicon nitride was deposited on the tunnel oxide as a charge-trapping layer, followed by deposition of a 20 nm HDPCVD silicon dioxide as the blocking oxide. The deposition of the HDPCVD silicon nitride was kept at 200°C in a low pressure of 3 mTorr with SiH4:NH3 = 12:24 sccm and an inductively coupled plasma (ICP) power of 900 W. The low pressure of 3 mTorr during deposition increases the path length an electron travels without undergoing a collision with a gas atom (or mean free path), which will improve the uniformity of the thin film.5 The blocking oxide was deposited at 350°C with SiH4:N2O = 6:150 sccm and a 900 W ICP power. Also, conventional LPCVD silicon nitride ONO gate stack was fabricated as a comparison. The deposition of the LPCVD silicon nitride was kept at 780°C in a 350 mTorr quartz furnace with SiH2Cl2:NH3 = 30:130 sccm. Finally, the Al gate was patterned and sintered to form a metal/oxide/nitride/oxide/silicon (MONOS) structure.

Results and Discussion

The nitride layer of a SONOS memory device was utilized to capture the injecting carriers from the channel, which cause a variation of the threshold voltage of the memory device. Figure 1a shows the band diagrams of the “write” and “erase” operation of the MONOS structure with different gate polarities. When the device is written, the electrons tunnel directly from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of the nitride layer. When the device is erased, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the nitride layer. The blocking oxide is utilized to prevent the carriers of the gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling. Figure 1b exhibits capacitance-voltage (C-V) hysteresis after the MONOS capacitor is performed by bidirectional sweeping from 12 to −12 V and in reverse. It is clearly shown in Fig. 1b that the threshold-voltage shift (memory window, $\Delta V_T$) of the MONOS structure of the HDPCVD SiNx is prominent. The threshold-voltage shift of the HDPCVD SiN x ONO stack, 5.3 V, is considerably larger than that of the LPCVD SiN x ONO stack, 3.2 V, after the 12 V write operation. To lower the operating voltage, the thickness of the nitride and blocking oxide layers should be reduced at the expense of decreasing the memory window. Although the threshold-voltage shift may be lower than that depicted above, a typical sense amplifier was designed to detect threshold-voltage differences as low as 50 mV.5 With the optimization of the thickness in the gate-stacked ONO structure, the low-voltage and reliable operation, lower than 5 V, is possible. The HDPCVD silicon nitride was produced in a high-density-plasma chamber with a 900 W ICP power. The radio frequency (rf) ICP power was used to increase the spiral motion of the charged particle. A charged particle gains more energy the more times it moves around the spiral and, hence, a high density plasma is produced.6 During deposition of the nitride layer, the simultaneously slight etching due to the bombardment of the high-density plasma is processed, which forms a densified and trap-rich silicon nitride layer.5,6


© 2004 The Electrochemical Society. [DOI: 10.1149/1.1695537] All rights reserved.

E-mail: tcchang@mail.phys.nsysu.edu.tw
LPCVD silicon nitride was deposited in a high-temperature furnace, which forms a well-bonded silicon nitride layer with fewer traps. In Fig. 2, Fourier transform infrared spectroscopy (FTIR) of the nitrides is shown schematically. A broadened peak of N-H bonding mode is obviously observed at the wavenumber of 3350 cm$^{-1}$ in the spectrum of HDPCVD nitride rather than the LPCVD one. Hydrogenated silicon nitride was formed due to the low-temperature deposition and the hydrogen cannot be completely outgassed as the high-temperature LPCVD nitride. The trap-rich HDPCVD SiN$_x$, therefore, results in a larger memory window ($\Delta V_t$) which probably makes the retention characteristics meet the 10 year tolerance.

The term “retention” describes the ability of the nonvolatile memory device to store and recover information after a number of program cycles at a specified temperature.$^{3,4}$ A premise for this attention is that the leakage behavior of the memory device should be tolerable. To maintain a good retention characteristic, the leakage current of the triple-dielectric ONO structure should be taken into account. Fortunately, as shown in Fig. 3, due to the well-densified silicon nitride layer,$^{6,7}$ the leakage current of the HDPCVD SiN$_x$ ONO structure is slightly higher than that of conventional LPCVD Si$_3$N$_4$ within an order of magnitude. The leakage characteristics are still within a superior range compared with a conventional approach. This property makes the HDPCVD silicon nitride a good candidate to replace the conventional nitride layer for providing a larger memory window.

To test the retention characteristics of our MONOS structure, a stricter environment of 150°C was prepared. In Fig. 4, the threshold-voltage hysteresis after the MONOS capacitor is performed by sweeping from 12 to $-12$ V and in reverse.

Figure 1. Band diagrams of the “write” and “erase” operation of the MONOS structure with different gate polarities. Inset is the ONO gate-stacked structure in this study. (b) C-V hysteresis after the MONOS capacitor is performed by sweeping from 12 to $-12$ V and in reverse.
voltage shift is measured with different periods of time when the samples are heated at 150°C. If there is any loss of the trapped charges after the 12 V write operation at 150°C as time passes, the threshold-voltage shift gradually decreases. The ONO stack of HD-PCVD silicon nitride retains good retention without a significant decline of the memory window up to 15 h, the same as a conventional LPCVD silicon nitride. This demonstrates the HDPCVD silicon nitride is robust enough to be adopted into SONOS EEPROM technology.

Conclusion

In this study, a MONOS structure of the HDPCVD silicon nitride was fabricated to replace the conventional LPCVD silicon nitride ONO stack. HDPCVD SiNx ONO stack, with a low leakage current, provides a larger memory window than the LPCVD Si3N4 ONO stack. Also, the retention characteristics was tested in a high-temperature environment of 150°C. The HDPCVD SiNx MONOS structure maintained a large memory window at 150°C up to 15 h. With the optimization of the thickness in the gate-stacked ONO structure, low-voltage and reliable operation, lower than 5 V, is realizable. It is concluded HDPCVD silicon nitride is robust enough to be a candidate for future SONOS EEPROM technology.

Acknowledgment

This work was performed at National Nano Device Laboratory and was supported by National Nano Device Laboratory under contract no. 92A0500001 and the National Science Council of the Republic of China under contract no. NSC92-2112-M-110-020 and NSC92-2215-E-110-006.

National Sun Yat-Sen University assisted in meeting the publication costs of the article.

References