Quasi-Superlattice Storage

A Concept of Multilevel Charge Storage


E-mail: tcchang@mail.phys.nsgu.edu.tw

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In this work, a novel concept of quasi-superlattice storage (QS\textsuperscript{2}) is demonstrated. Under a suitable operating voltage, two apparent states of charge storage can be distinguished. The memory effects are due to the multilevel charge storage within the quasi-superlattice. The multilevel charge storage provides a feasible design for the 2-bit-per-cell nonvolatile memory devices. Also, the leakage behavior of the quasi-superlattice structure has also been characterized by current-voltage measurements at room temperature and low temperatures. The resonant tunneling-like leakage characteristic is observed at low temperatures. A concise physical model is proposed to characterize the leakage mechanism of tunneling for the quasi-superlattice structure, and this suggests that consideration of the operating voltage for the 2-bit-per-cell nonvolatile memory device needs to be taken into account.

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Recently, portable electronic devices, such as digital cameras, laptops, smart cards, mp3 players, USB FLASH, have received much attention in the market place and have significantly impacted the semiconductor industries. All the above mentioned products are based on the device of FLASH nonvolatile memory. The commercially available FLASH memory contains the structure of a polysi floating gate (FG), which serves as a charge-trapping layer. Since the difficulties of consecutive scaling have been addressed,\textsuperscript{2} the candidate, silicon-oxide-nitride-silicon (SONOS) nonvolatile memory device, is now in the position to become an important part of the industry.\textsuperscript{3,4} SONOS possesses a structure similar to the FG memory device but silicon nitride rather than polysi is adopted as the charge-trapping layer.\textsuperscript{5,6} The SONOS structure has a great potential of scaling the thickness of the tunnel oxide down to 1.6 nm and reducing the programming voltage below 5 V.\textsuperscript{7,9} That, hence, improves the speed of performance of the memory device.\textsuperscript{10} In this study, both Si and silicon nitride are utilized as the charge-trapping layers and a Si/silicon nitride quasi-superlattice structure is proposed as the multilevel charge storage for the first time. A 2-bit per cell Fowler-Nordheim (F-N) tunneling operation has been proposed for the electrical measurements. The leakage behavior of the quasi-superlattice stack for the multilevel charge storage has also been demonstrated and a concise model is proposed to derive and explain the leakage behavior of the quasi-superlattice gate stack.

Experimental

Single-crystal, 6 in. diam, (100) oriented p-type silicon wafers were used in the present study. The wafers were chemically cleaned by a standard RCA cleaning, followed by a dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace at 925°C to form a 3 nm tunnel oxide. Subsequently, silicon nitride (Si\textsubscript{3}N\textsubscript{4}) and amorphous Si (a-Si) quasi-superlattice of two periods were deposited by low pressure chemical vapor deposition (LPCVD) at 780 and 550°C, respectively. Each of the four LPCVD layers was controlled to be about 2 nm. A 10 nm thick tetraethyl-orthosilicate (TEOS) oxide was deposited on the QS\textsuperscript{2} as the control oxide layer. To densify the two a-Si layers, a steam densification, the two a-Si layers were crystallized into microcrystals or polycrystals, which depends on the grain size of the Si layers. After the Al electrodes were patterned and sintered, capacitance-voltage (C-V) measurements were performed to investigate the memory effects of the quasi-superlattice storage (QS\textsuperscript{2}) memory device.

Results and Discussion

Figure 1 shows the device structure in this work. The quasi-superlattice of Si\textsubscript{3}N\textsubscript{4} and a-Si, sandwiched between the tunnel oxide and the control oxide, is utilized as a charge storage element for a memory device instead of polysi FG or Si\textsubscript{3}N\textsubscript{4} single layer. Figure 2 shows the ideal energy band diagram of the QS\textsuperscript{2} memory device at V = 0. The quasi-superlattice of Si\textsubscript{3}N\textsubscript{4} and a-Si clearly shows the band offsets that can easily trap electrons as the storage elements. The undoped a-Si layers are with a wider bandgap than that of the Si substrate. To write the memory device, a positive gate voltage has to be applied to make electrons directly tunnel through the tunnel oxide by F-N tunneling. The tunneling electrons may be trapped in the trap states of the nitride layers, the interface states between Si\textsubscript{3}N\textsubscript{4} and a-Si layers, or the quantum wells of the a-Si layers. The trapped electrons cause a threshold voltage shift (\Delta V\textsubscript{T}), memory window, of the memory device, which can be defined as 1 or 0, according to the different threshold voltages. To erase the memory device, negative gate polarity is applied to make the trapped electrons tunnel back to the channel. The control oxide is utilized to prevent the carriers of the gate electrode from injecting into the charge trapping sites by F-N tunneling.

Figure 3 exhibits C-V hysteresis after the bidirectional voltage sweeping. The voltage is swept between 4 and (−7) V or 7 and (−7) V. The erasing voltage is fixed at −7 V. Under the programming voltage of 4 and 7 V, the memory window is 0.1 and 0.93 V, respectively, and increases with the programming voltage. It is worth noting that the hysteresis is counterclockwise which is due to substrate injection from the electrons of the deep inversion layer and holes of the deep accumulation layer of the Si substrate.\textsuperscript{11}

Under varied programming voltages and fixed erasing voltage, the relationship between the threshold voltage shift and programming voltage is of special interest. Figure 4 exhibits the gate voltage dependence of the memory window. The threshold voltage shift is increased with the gate voltage. However, two sudden rises of the threshold voltage shift are observed, which take place around 5 and 9.5 V. As the memory device is written with different programming voltages, the tunneling electrons will be captured at the trap states of the Si\textsubscript{3}N\textsubscript{4} layer, the interface states between Si\textsubscript{3}N\textsubscript{4} and a-Si layers, and/or the quantum well of a-Si. During low-voltage programming, the electrons are captured at the charge-trapping sites of trap states of the Si\textsubscript{3}N\textsubscript{4} layer and the interface states between Si\textsubscript{3}N\textsubscript{4} and a-Si layers. The sudden rise implies the charge storage of the a-Si quan-
tum well. Figure 5 shows the programmed band diagram of the memory device. The first sudden rise in Fig. 4 is attributed to the charge storage in the a-Si quantum well between two nitride layers. The second sudden rise is deduced to be that occurring under high-voltage programming when the electrons may be written in to the a-Si quantum well between nitride and control oxide layers. It is also observed that in Fig. 4 the increments of the two sudden rises are obviously different from each other. The increment of the second sudden rise is smaller than that of the first one. The threshold voltage shift is due to the electrons trapped in the gate dielectrics, and the trapped electrons away from the channel influence the threshold voltage less. Therefore, a larger threshold voltage shift is observed among the first low-voltage charge storage in the a-Si quantum well. The threshold voltage of a metal-oxide-semiconductor (MOS) capacitor is described as

\[ V_t = V_{FB} + 2\phi_B + \frac{\sqrt{4\varepsilon_S q N_A \phi_B}}{C_i} \]  

where \( V_{FB} \) is the flatband voltage shift; \( \phi_B \), the potential difference between the Fermi level, \( E_F \), and the intrinsic Fermi level, \( E_i \); \( \varepsilon_S \), the permittivity of the semiconductor; \( N_A \), the density of the acceptors; and \( C_i \), the capacitance of the insulator. In this study, the threshold voltage shift, \( \Delta V_t \), is mainly determined by the flatband voltage shift, \( \Delta V_{FB} \), \( \Delta V_t \approx \Delta V_{FB} = Q_t/C_i \), where \( Q_t \) is the charge trapped in the quasi-superlattice structure after programming. As inferred in Fig. 4, the trapped charge \( Q_t \) is increased with the programming voltage. Under low-voltage programming below 5 V, the injecting charges can tunnel through the tunnel oxide and be trapped in the forbidden gap of the first nitride layer and the interface between Si and Si\(_3\)N\(_4\). It is not easy for the electrons to cross

\[ \frac{\Delta V_t}{\Delta V_{FB}} = \frac{Q_t}{C_i} \]

Figure 3. C-V hysteresis after the bidirectional voltage sweep. The erasing voltage is fixed at \((-7)\) V.

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![Figure 1](image1.png)

**Figure 1.** The cross-sectional figure of the quasi-superlattice structure.

![Figure 2](image2.png)

**Figure 2.** The ideal energy band diagram of the QS\(^2\) memory device at \( V = 0 \).

![Figure 3](image3.png)

**Figure 3.** C-V hysteresis after the bidirectional voltage sweep. The erasing voltage is fixed at \((-7)\) V.

![Figure 4](image4.png)

**Figure 4.** Gate voltage dependence on the memory window. There are two sudden rises of the threshold voltage shift observed, which take place at around 5 and 9.5 V.
implies a 2-bit-per-cell operation by F-N tunneling. In the design of the multilevel storage, the initial threshold voltage shift is needed to lead to the second rise of the memory window. Beyond the programming voltage of 7 V, the increased memory window is attributed to the charge storage in the forbidden gap of the second nitride layer, overcoming the barrier height of ~2.0 eV between Si and the nitride. The programming voltage of 9.5 V and above is needed to lead to the second rise of the threshold voltage shift. In this work, the quasi-superlattice storage stack structure, current-voltage electrical measurements are performed. Figure 6 exhibits the current density-voltage (J-V) characteristics for both room temperature and 50 K. The inset shows the local amplification of the J-V curve at 50 K.

Figure 5. The band diagram of the memory device under programming. Under suitable operating voltages, two apparent states of charge storage can be distinguished.

To investigate the leakage behavior of the quasi-superlattice stack structure, the leakage current-voltage characteristics are performed. Figure 6 exhibits the current density-voltage (J-V) characteristics for both room temperature and 50 K. The inset shows the local amplification of the J-V curve at 50 K. The negative differential resistance occurs at around 5.2 V. The peak current density at 7 V in Fig. 6 is inferred to be the resonant tunneling of E2 between the two a-Si quantum wells. During the temperature operation, the leakage behavior is dominated by the tunneling effects which can be described as $J = \frac{n^2 \pi^2 h^2}{2m^* L^2} \exp[-C/V]$, where $V$ is the programming voltage and $C$ is a constant. Considering the quantum confinement of the Si quantum wells, the energy levels are defined as $E_n = \frac{n^2 \pi^2 h^2}{2m^* L^2}$, where $n = 1, 2, 3, ..., m^*$ is the effective mass of the electrons in the quantum well.

Figure 6. The current J-V characteristics for both room temperature and 50 K. The inset shows the local amplification of the J-V curve at 50 K.

Figure 7. The ideal energy band diagram of the quasi-superlattice stack under zero bias with split energy levels.
superlattice structure, and \( L \) is the thickness, −2 nm, of the Si quantum wells. As \( n = 1, 2, \) and \( 3 \), \( E = E_1, E_2, \) and \( E_3 \), the resonant tunneling occurs at the programming voltage of \( 2, 5.2, \) and \( 7 \) V, respectively. To calculate the resonant voltage drop of the Si quantum wells, \( m^* \) is estimated to be around \( 0.19 m_0 \) for the electrons transported in the Si layer. The first resonant tunneling voltage drop \( V_{1t} \) of the Si quantum wells can be calculated by \( V_{1t} = 2E_1/q \approx 0.98 \) V, where \( q = 1.6 \times 10^{-19} \) C. Also, \( V_{2t} \) and \( V_{3t} \) can be calculated as \( V_{2t} = 3.92 \) V and \( V_{3t} = 8.82 \) V. The first resonant tunneling is occurs when the programming voltage reached about \( 2 \) V. Therefore, the voltage difference of \( 2 - 0.98 = 1.02 \) V is dropped on the tunnel oxide, control oxide, and nitride layers. To motivate the second resonant tunneling, additional voltage is dropped on the Si quantum wells, \( V_{2t} - V_{1t} \), needs to be supplied. The additional voltage drop is calculated as 2.94 V, which is close enough to the voltage difference, 3.2 V, of the programming voltage between first and second resonant tunneling. As the programming voltage is increased to 7 V to stimulate the third resonant tunneling, it is deduced that the third resonant tunneling is due to the instability of the two amorphous silicon layers where there should be at least 8.82 V to motivate the third resonant tunneling between the Si quantum wells. The investigation of the leakage mechanism of the quasi-superlattice stack will help the multilevel charge storage develop the considerations of operating voltage for the 2-bit-per-cell nonvolatile memory device. Further study about the reliability characteristics is being taken into account and is currently under investigation.

Conclusions

In this study, a novel quasi-superlattice storage has been demonstrated for the concept of multilevel charge storage. In the relationship between threshold voltage shift and gate programming voltage, two sudden rises were observed. The obvious memory effects from the measurements of C-V hysteresis exhibited two distinguishable charge storages, which can be utilized as a memory device of 2-bit-per-cell. The study on the leakage behavior of the quasi-superlattice stack has also been demonstrated for room temperature and low temperature. The current-voltage characteristics of the quasi-superlattice structure behave like those of the resonant tunneling diode at low temperatures. The negative differential resistance occurs at around 2, 5.2, and 7 V. A concise model is proposed to understand the leakage behavior of the quasi-superlattice stack.

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