Memory characteristics of Co nanocrystal memory device with HfO$_2$ as blocking oxide

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In this letter, we demonstrated the electron charging and discharging effects of Co nanocrystals embedded in SiO$_2$ and HfO$_2$, which is desirable for applications of the nonvolatile memory technology. Its implementation is compatible with the current manufacturing technology of semiconductor industry.

Nonvolatile memory devices with floating-gate structure are being used widely, for example, in mp3 players, digital cameras, and integrated circuit cards at present. The most prominent one is the limited potential for continued scaling of the device structure. When the tunnel oxide is thinner, the retention characteristics may be degraded, and when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. There is, therefore, a trade-off between speed and reliability and the thickness of the tunnel oxide is compromised to about 8–11 nm, which is barely reduced over more than five generations of the industry. Recently, memory-cell structure using discrete traps as the charge storage media has received much attention as the promising candidate to replace conventional dynamic random access memory or flash memories for future high speed and low power consuming memory devices. Among the different materials of nanocrystals, the metal nanocrystal memory possesses several advantages, such as stronger coupling with the conduction channel, a wide range of available work functions, higher density of states around the Fermi level, and smaller energy perturbation due to carrier confinement. Besides, using the high-$k$ dielectric as the blocking oxide concentrates and releases the electric fields across the tunnel oxide and the blocking oxide, respectively, under the program/erase mode. Using the high-$k$ dielectric as the blocking oxide leads to lower program and erase voltage.

In this letter, we demonstrated the electron charging and discharging effects of Co nanocrystals embedded in SiO$_2$ and HfO$_2$, which is desirable for applications of the nonvolatile memory technology. Its implementation is compatible with the current manufacturing technology of semiconductor industry.

(100) oriented $p$-type silicon wafers were chemically cleaned by a standard Radio Corporation of America cleaning, followed by thermally growing of a 3 nm tunnel oxide at 1000 °C in a vertical furnace system. Subsequently, a 3-nm-thick cobalt layer was deposited onto the tunnel oxide by electron beam evaporation. The Co nanocrystals were formed by rapid thermal annealing in the N$_2$ ambient at 500 °C for 60 s. The 30-nm-thick blocking oxide (HfO$_2$) was capped by sputtering. Finally, Al gate electrode was patterned and sintered. The structural analyses were performed by transmission electron microscopy (TEM). The capacitance-voltage (C-V) measurements were performed by an HP 4284A precision LCR meter to study the electron charging and discharging effects of the Co nanocrystals.

Figure 1 presents typical bright-field, cross-section TEM images. It shows the structure of HfO$_2$/Co/SiO$_2$/Si. As il-
Illustrated in Fig. 1, the well-separated and spherical Co nanocrystals embedded between the SiO\textsubscript{2} layer and HfO\textsubscript{2} layers were observed. The aerial density and mean size of the Co nanocrystals are measured to be $2.13 \times 10^{12}/\text{cm}^2$ and 2 nm, respectively.

Figure 2(a) shows the forward and reverse sweep C-V characteristics, indicating the electron charging and discharging effects of Co nanocrystals embedded between the SiO\textsubscript{2} and HfO\textsubscript{2} layers. The bidirectional C-V sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited electron charging effect. In Fig. 2(a), with the voltage swept from 5 to $-5$ V and back to 5 V, an outstanding threshold voltage shift of 1 V was observed. As the whisked voltage was increased to 7 V, a more obvious C-V shift of 1.8 V was seen. It is perceived that the hysteresis is counterclockwise which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate. The result of C-V shift indicates that the charging effects of Co nanocrystals are more significant than those of the semiconductor nanocrystals. The high-k blocking oxide concentrates the electric fields across the tunnel oxide and releases it across the blocking oxide under program and erase mode. This effect leads to lower program and erase voltage. Figure 2(b) shows the band diagrams of “program” and “erase” operations with different gate polarities of the memory device. When the device is written or programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide and are trapped in the Co nanocrystals. On the other hand, as the device is erased, the electrons may tunnel back to the deep accumulation layer of Si substrate. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the Co nanocrystals by Fowler-Nordheim tunneling. In addition, the Co nanocrystals do not bear a voltage drop from gate voltage, which means that all the voltages provided from control gate are dropped to the tunnel oxide and control oxide and gain advantage over their semiconductor counterparts. The operating voltage of the memory devices with conventional floating gate or semiconductor nanocrystals embedded in SiO\textsubscript{2} is above 7 V. In our approach to fabricate the Co nanocrystals embedded in SiO\textsubscript{2}, a lower programming voltage of 5 V and erasing voltage of $-5$ V realize a significant threshold voltage shift, 1 V, which is sufficient to be defined as “1” and “0” by a typical sensing amplifier for a memory device.

The retention characteristics of the Co nanocrystals were measured at room temperature, as shown in Fig. 3. If there are some leakage paths for the trapping charges, the memory effect will gradually decrease. In Fig. 3, the good retention characteristics and the memory effect without significant decreasing up to $10^4$ s can be founded. The charge loss rate only decreases to 21.95% after $10^4$ s. The inset shows that the threshold voltage shift does not significantly decrease after a long time ($10^4$ s). It is clearly shown that the Co nanocrystal memory has excellent retention characteristic.

In addition, the reliability of the memory device was also investigated. As shown in Fig. 4, the data endurance of the Co nanocrystal memory device retains an obvious memory window of 0.86 V after $10^6$ cycles and write/erase voltage was $5/(-5)$ V. The good endurance behavior of the Co nanocrystal memory device can be founded.
In summary, the memory effects of the Co nanocrystals using tunneling and control oxides, SiO₂ and HfO₂, were demonstrated in this letter. A significant C-V hysteresis of Vₜ shift of 1 V is observed under the low operating voltage of 5 V. The retention characteristics are tested to be robust. Also, the endurance of the memory device is not degraded up to 10⁶ write/erase cycles.

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